

Preliminary Amendment

Page 4 of 4

Applicants: Sinha et al

Serial No. 10/028,040

Filed: December 21, 2001

For: METHODS FOR PLANARIZATION OF GROUP VIII METAL-CONTAINING SURFACES USING
COMPLEXING AGENTS

Remarks

The specification has been amended to include application serial numbers, to remove attorney docket numbers, and to correct typographical errors. No new matter has been added as a result of these amendments.

Conclusion

The Examiner is invited to contact Applicants' Representatives at the below-listed telephone number, if there are any questions regarding this Preliminary Amendment or if prosecution of this application may be assisted thereby.

Respectfully submitted for

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper is being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 2327, Arlington, VA 22202, on this 19 day of July, 2002.

Ann M. Mueting
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APPENDIX A - SPECIFICATION/CLAIM AMENDMENTS
INCLUDING NOTATIONS TO INDICATE CHANGES MADE

Serial No.: 10/028,040
Docket No.: 150.01140101

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Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted. Additionally, all amendments have been shaded.

In the Specification

The paragraph beginning at page 13, line 11, has been amended as follows:

For various desired effects, a planarization composition can optionally and preferably include an oxidizing agent to aid in the planarization. Examples of suitable planarization compositions are disclosed in Applicant's Assignee's copending U.S. Patent Applications: Serial Number [] **10/028,249**, filed on [even date herewith] **December 21, 2001** entitled METHODS FOR PLANARIZATION OF GROUP VIII METAL-CONTAINING SURFACES USING OXIDIZING AGENTS [(Atty. Docket No. **150.01050101**)]; and Serial Number [] **10/032,357**, filed on [even date herewith] **December 21, 2001** entitled METHODS FOR PLANARIZATION OF GROUP VIII METAL-CONTAINING SURFACES USING OXIDIZING GASES [(Atty. Docket No. **150.01110101**)].

The paragraph beginning at page 17, line 17, has been amended as follows:

The figures provide further information about the methods of the invention. Figure 1A illustrates one portion of a wafer 10 prior to planarization in accordance with the present invention having features that are filled with the material to be removed through planarization. The wafer portion 10 includes a substrate assembly 12 having junctions 16 formed thereon. A capacitor and/or barrier layer material 19 is then formed over the substrate assembly 12 and the junctions 16. The [a] capacitor and/or barrier layer material 19 may be any conductive material such as platinum or any other suitable conductive second or third row Group VIII metal-containing capacitor and/or barrier material. Generally, as shown in Figure 1A, the nonplanar upper surface 13 of capacitor and/or barrier layer 19 is subjected to planarization or other processing in accordance with the present invention. The resulting wafer 10, which is



Preliminary Amendment - Appendix A

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Page 2 of 3
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shown in Figure 1B, includes an upper surface 17 planarized such that the thickness of the wafer 10 is substantially uniform across the entire wafer 10 so that the wafer now includes a capacitor and/or barrier structure layer 14.

The paragraph beginning at page 18, line 4, has been amended as follows:

Figure [2B] 2A illustrates one portion of a wafer 20 prior to planarization in accordance with the present invention having features that have a conformal layer of the material to be removed through planarization. The wafer portion 20 includes a substrate assembly 22 having a patterned dielectric layer 26 formed thereon. Such a patterned dielectric layer 26 can be used in a variety of structures, particularly a capacitor structure. The patterned dielectric layer 26 can be formed of any material that provides electrical isolation between metal regions (e.g., silicon dioxide, silicon nitride, or BPSG). An electrode layer 29 is then formed over the substrate assembly 22 and the patterned dielectric layer 26. The electrode layer 29 may be platinum or any other suitable conductive second or third row Group VIIIB or Group IB metal-containing material. Generally, as shown in Figure 2A, the nonplanar upper surface 23 of electrode layer 29 is subjected to planarization or other processing in accordance with the present invention. The resulting wafer 20, as shown in Figure 2B, includes an upper surface 27 planarized such that the thickness of the wafer 20 is substantially uniform across the entire wafer 20 so that the wafer now includes electrically conducting regions 24 isolated within the patterned dielectric material 26 forming a capacitor structure. If desired, prior to planarization, the conformal layer 29 and openings 24 can be covered with a photoresist or other material that is removed after the planarization so the abrasive does not fall into the openings 24.